

WHAT IS CLAIMED IS:

1. A method of testing a transceiver circuit, the method comprising:
receiving serial test data via a receiver serial input port;
converting the serial test data into parallel test data using at least a
portion of a receiver circuit in a normal operation mode;
in response to a test command, coupling the parallel test data to an
internal transmitter circuit parallel input port, thereby bypassing an externally
accessible transmitter parallel data input used in the normal operation mode;
in response to the test command, coupling a receiver clock signal
recovered from the serial test data by the receiver circuit to at least a portion of a
transmitter circuit, thereby bypassing a reference clock used in the normal
operation mode by the portion of the transmitter circuit;
converting the parallel test data into serial output data using at least the
portion of transmitter circuit in the normal operation mode; and
providing the serial output data to a transmitter serial output port,
wherein the serial output data can then be analyzed.

2. The method as defined in Claim 1, wherein the parallel test data is
provided to a multiplexer which selectively couples one of the parallel test data and the
data received via the externally accessible transmitter parallel data input to the internal
transmitter circuit parallel input port based on a state of a test command signal.

3. The method as defined in Claim 1, wherein the portion of the transmitter
circuit includes a transmitter clock multiplier circuit.

4. The method as defined in Claim 1, further comprising performing a
phase alignment on the parallel test data using a transmitter phase alignment circuit.

5. The method as defined in Claim 1, wherein the parallel test data has been
synchronized with the receiver clock and aligned by the receiver circuit.

6. The method as defined in Claim 1, wherein the act of converting the
parallel test data into serial output data further comprises multiplexing the parallel test
data into the serial output data using the reference clock.

7. The method as defined in Claim 1, further comprising generating the
serial test data using test equipment.

8. The method as defined in Claim 1, further comprising reading the serial output data using test equipment.

9. A transceiver, including a built in test circuit, comprising:

a test control input configured to receive a test control signal;

5 a receiver serial input port configured to receive externally supplied serial data;

a receiver circuit coupled to the receiver serial input port to receive the externally supplied serial data, the receiver circuit configured to convert the externally supplied serial data into parallel data, and to generate a receiver clock based at least in part on the externally supplied serial data;

10 a reference clock circuit configured to generate a reference clock;

a transmitter parallel input port having an input and an output, the input port configured to receive externally supplied parallel data;

15 a first multiplexer circuit having a first input port coupled to the receiver circuit so as to receive the parallel data from the receiver circuit, a second input port coupled to the parallel input port output to receive the externally supplied parallel data, a first multiplexer output port, and a first control input coupled to the test control input, wherein the first multiplexer circuit selectively couples one of the multiplexer first port and the multiplexer second port to the first multiplexer output port to provide corresponding parallel data in response to the test control signal;

20 a second multiplexer circuit having a third input port coupled to the receiver circuit so as to receive the receiver clock, a fourth input port coupled to the reference clock circuit to receive the reference clock, a second multiplexer output port, and a second control input coupled to the test control input, wherein the second multiplexer circuit selectively couples one of the multiplexer first port and the multiplexer second port to the second multiplexer output port to provide a corresponding clock in response to the test control signal;

25 a transmitter circuit coupled to the first multiplexer output and the second multiplexer output, wherein the transmitter circuit is configured to convert the corresponding parallel data received from the first multiplexer output

to transmitter serial data, the transmitter circuit further configured to use the corresponding clock from the second multiplexer output to process the corresponding parallel data; and

a transmitter output port coupled to the transmitter circuit to receive the transmitter serial data.

10. The transceiver as defined in Claim 9, wherein the transmitter circuit further comprises a clock multiplier circuit configured to receive the corresponding clock;

11. The transceiver as defined in Claim 9, wherein the receiver circuit is configured to synchronize the parallel data with one of the receiver clock and the reference clock.

12. The transceiver as defined in Claim 9, wherein the receiver circuit is configured to align the parallel data.

13. A testing system, comprising:

a test control input configured to receive a test control signal;

a receiver serial input port configured to receive externally supplied serial data;

a receiver circuit coupled to the receiver serial input port to receive the externally supplied serial data, the receiver circuit configured to convert the externally supplied serial data into parallel data, and to generate a receiver clock based at least in part on the externally supplied serial data;

a reference clock circuit configured to generate a reference clock;

a transmitter parallel input port having an input and an output, the input port configured to receive externally supplied parallel data;

a first multiplexer circuit having a first input port coupled to the receiver circuit so as to receive the parallel data from the receiver circuit, a second input port coupled to the parallel input port output to receive the externally supplied parallel data, a first multiplexer output port, and a first control input coupled to the test control input, wherein the first multiplexer circuit selectively couples one of the multiplexer first port and the multiplexer second port to the first

multiplexer output port to provide corresponding parallel data in response to the test control signal;

5 a second multiplexer circuit having a third input port coupled to the receiver circuit so as to receive the receiver clock, a fourth input port coupled to the reference clock circuit to receive the reference clock, a second multiplexer output port, and a second control input coupled to the test control input, wherein the second multiplexer circuit selectively couples one of the multiplexer first port and the multiplexer second port to the second multiplexer output port to provide a corresponding clock in response to the test control signal;

10 a transmitter circuit coupled to the first multiplexer output and the second multiplexer output, wherein the transmitter circuit is configured to convert the corresponding parallel data received from the first multiplexer output to transmitter serial data, the transmitter circuit further configured to use the corresponding clock from the second multiplexer output to process the corresponding parallel data;

15 a transmitter output port having coupled to the transmitter circuit to receive the transmitter serial data from the transmitter circuit and to provide the serial data; and

20 test equipment coupled to the test control input, the receiver serial input port, and the transmitter output port, the test equipment configured to generate the externally supplied serial data and the test control signal, the test equipment further configured to receive the transmitter serial data from the transmitter output port.